Optimizing polarization-diversity couplers for Si-photonics: reaching the -1dB coupling efficiency threshold

Lee Carroll,[1] Dario Gerace,[1] Ilaria Cristiani,[2] and Lucio C. Andreani[1]

[1]*Department of Physics, University of Pavia, Via Bassi 6, I-27100 Pavia, Italy*
[2]*Department of Electrical, Computer and Biomedical Engineering, University of Pavia, Via Ferrata 1, I-27100 Pavia, Italy*
[*]*lee.carroll@unipv.it*

Abstract: Polarization-diversity couplers are low-cost industrially-scalable passive devices that can couple light of unknown polarization from a telecom fiber-mode to a pair of TE-polarized wave-guided modes in the Silicon-on-Insulator platform. These couplers offer significantly more relaxed alignment tolerances than edge-coupling schemes, which is advantageous for commercial fiber-packaging of Si-photonic circuits. However, until now, polarization-diversity couplers have not offered sufficient coupling efficiency to motivate serious commercial consideration. Using 3D finite difference time domain calculations for device optimization, we identify Silicon-on-Insulator polarization-diversity couplers with 1550nm coupling efficiencies of −0.95dB and −1.9dB, for designs with and without bottom-reflector elements, respectively. These designs offer a significant improvement over state-of-the-art performance, and effectively bridge the "performance gap" between polarization-diversity couplers and 1D-grating couplers. Our best polarization-diversity coupler design goes beyond the −1dB efficiency limit that is typically accepted as the minimum needed for industrial adoption of coupler devices in the telecoms market.

OCIS codes: (050.1755) Computational electromagnetic methods; (050.5298) Photonic crystals; (130.1750) Components; (130.5440) Polarization-selective devices.

References and links

1. T. Baehr-Jones, T. Pinguet, P. L. Guo-Qiang, S. Danziger, D. Prather, and M. Hochberg, "Myths and rumours of silicon photonics," Nat. Photonics **6**(4), 206–208 (2012).
2. M. Streshinsky, R. Ding, Y. Liu, A. Novack, C. Galland, A. Lim, P. Guo-Qiang Lo, T. Baehr-Jones, and M. Hochberg, "The Road to Affordable, Large-Scale Silicon Photonics," Opt. Photon. News **24**(9), 32–39 (2013).
3. C. Kopp, S. Bernabé, B. Bakir, J.-M. Fedeli, R. Orobtchouk, F. Schrank, H. Porte, L. Zimmermann, and T. Tekin, "Silicon photonic circuits: on-CMOS integration, fiber optical coupling, and packaging," IEEE J. Sel. Top. Quantum Electron. **17**(3), 498–509 (2011).
4. S. Pathak, M. Vanslembrouck, P. Dumon, D. Van Thourhout, and W. Bogaerts, "Compact SOI-based polarization diversity wavelength de-multiplexer circuit using two symmetric AWGs," Opt. Express **20**(26), B493–B500 (2012).
5. X. Chen and H. K. Tsang, "Polarization-independent grating couplers for silicon-on-insulator nanophotonic waveguides," Opt. Lett. **36**(6), 796–798 (2011).
6. W. S. Zaoui, A. Kunze, W. Vogel, and M. Berroth, "CMOS-compatible polarization splitting grating couplers with a backside metal mirror," IEEE Photon. Technol. Lett. **25**(14), 1395–1397 (2013).
7. B. Charbonnier, S. Menezo, P. O'Brien, A. Lebreton, J. Fedeli, and B. Ben Bakir, "Silicon photonics for next generation FDM/FDMA PON," J. Opt. Commun. Netw. **4**(9), A29–A37 (2012).
8. W. Bogaerts, D. Taillaert, B. Luyssaert, P. Dumon, J. Van Campenhout, P. Bienstman, D. Van Thourhout, R. Baets, V. Wiaux, and S. Beckx, "Basic structures for photonic integrated circuits in Silicon-on-insulator," Opt. Express **12**(8), 1583–1591 (2004).

#210055 - $15.00 USD Received 14 Apr 2014; revised 13 May 2014; accepted 14 May 2014; published 9 Jun 2014

9. D. Taillaert, F. Van Laere, M. Ayre, W. Bogaerts, D. Van Thourhout, P. Bienstman, and R. Baets, "Grating couplers for coupling between optical fibers and nanophotonic waveguides," Jpn. J. Appl. Phys. **45**(8A), 6071–6077 (2006).
10. D. Vermeulen, S. Selvaraja, P. Verheyen, G. Lepage, W. Bogaerts, and G. Roelkens, "High-efficiency silicon-on-insulator fiber-to-chip grating couplers using a silicon overlay," Group IV photonics, United States, FPd1 (2009).
11. C. Xia, L. Chao Li, C. K. Y. Fung, S. M. G. Lo, and H. K. Tsang, "Apodized waveguide grating couplers for efficient coupling to optical fibers," IEEE Photon. Technol. Lett. **22**(15), 1156–1158 (2010).
12. W. S. Zaoui, A. Kunze, W. Vogel, M. Berroth, J. Butschke, F. Letzkus, and J. Burghartz, "Bridging the gap between optical fibers and silicon photonic integrated circuits," Opt. Express **22**(2), 1277–1286 (2014).
13. D. Taillaert, H. Chong, P. I. Borel, L. H. Frandsen, R. M. De La Rue, and R. Baets, "A compact two-dimensional grating coupler used as a polarization splitter," IEEE Photon. Technol. Lett. **15**(9), 1249–1251 (2003).
14. W. Bogaerts, D. Taillaert, P. Dumon, D. Van Thourhout, R. Baets, and E. Pluk, "A polarization-diversity wavelength duplexer circuit in silicon-on-insulator photonic wires," Opt. Express **15**(4), 1567–1578 (2007).
15. F. Van Laere, W. Bogaerts, P. Dumon, G. Roelkens, D. Van Thourhout, and R. Baets, "Focusing polarization diversity grating couplers in silicon-on-insulator," J. Lightwave Technol. **27**(5), 612–618 (2009).
16. L. Carroll, D. Gerace, I. Cristiani, S. Menezo, and L. C. Andreani, "Broad parameter optimization of polarization-diversity 2D grating couplers for silicon photonics," Opt. Express **21**(18), 21556–21568 (2013).
17. F. Van Laere, T. Stomeo, D. Taillaert, G. Roelkens, D. Van Thourhout, T. F. Krauss, and R. Baets, "Efficient polarization diversity grating couplers in bonded InP-membrane," IEEE Photon. Technol. Lett. **20**(4), 318–320 (2008).
18. A. Mekis, S. Gloeckner, G. Masini, A. Narasimha, T. Pinguet, S. Sahni, and P. De Dobbelaere, "A grating-coupler-enabled CMOS photonics platform," IEEE J. Sel. Top. Quantum Electron. **17**(3), 597–608 (2011).
19. D. Vermeulen, S. Selvaraja, P. Verheyen, G. Lepage, W. Bogaerts, P. Absil, D. Van Thourhout, and G. Roelkens, "High-efficiency fiber-to-chip grating couplers realized using an advanced CMOS-compatible Silicon-On-Insulator Platform," Opt. Express **18**(17), 18278–18283 (2010).
20. G. Roelkens, D. Van Thourhout, and R. Baets, "High efficiency Silicon-on-Insulator grating coupler based on a poly-Silicon overlay," Opt. Express **14**(24), 11622–11630 (2006).
21. S. K. Selvaraja, D. Vermeulen, M. Schaekers, E. Sleeckx, W. Bogaerts, G. Roelkens, P. Dumon, D. Van Thourhout, and R. Baets, "Highly Efficient Grating Coupler between Optical Fiber and Silicon Photonic Circuit," in "Conference on Lasers and Electro-Optics/International Quantum Electronics Conference," (Optical Society of America), OSA Technical Digest, CTuC6 (2009).
22. M. Popovic, T. Barwicz, M. S. Dahlem, F. Gan, C. W. Holzwarth, P. T. Rakich, H. I. Smith, E. P. Ippen, and F. X. Krtner, "Tunable, Fourth-Order Silicon Microring-Resonator Add-Drop Filters," 33rd European Conference and Exhibition of Optical Communication (ECOC), 1–2 (2007).
23. L. C. Andreani and D. Gerace, "Photonic crystal slabs with a triangular lattice of triangular holes investigated using a guided mode expansion method," Phys. Rev. B **73**(23), 235114 (2006).

1. Introduction

The last decade has seen a strong push towards developing integrated silicon photonic circuits for information and communication technology (ICT). Combining low-cost complementary metal oxide semiconductor (CMOS) fabrication technology, with high transmission and high refractive index contrast, the SOI (silicon–on-insulator) platform has emerged as a principle Si-photonic architecture. Recently, there has been a significant research effort towards integrating individual Si-photonic devices to realize useful and commercially-orientated Si-photonic circuits [1, 2]. One on-going challenge in this field is to identify the best low-cost and industrially-scalable means of coupling light from a standard telecom fibre to a Si-photonic circuit with acceptably "high" coupling efficiency. Here, the problem is two-fold – (i) the mean-field diameter of the fibre-mode is about 10μm, while the standard SOI waveguide cross-section is 500nm × 220nm, and (ii) the polarization-state of the fibre-mode is generally unknown and unstable, while most Si-photonic circuits are designed for one particular polarization. One CMOS-compatible solution to bridging the dimensional gap between fibre and SOI-waveguide is a grating-coupler. The periodic structure of the grating-coupler is designed to create a diffraction condition that couples light from the near-normally incident light of the 10 μm fibre-mode into 220nm taper-waveguides etched into the horizontal plane of the SOI wafer. Essentially the periodicity of the grating-coupler creates a condition that adds a new effective *k*-vector to that of the incident fibre-mode, such that the resulting coupled-mode propagates in the horizontal plane, and is wave-guided by the Si-layer of the SOI-wafer. When properly optimized, grating-couplers provide both high coupling

#210055 - $15.00 USD Received 14 Apr 2014; revised 13 May 2014; accepted 14 May 2014; published 9 Jun 2014

efficiencies, and a relaxed alignment tolerance that can be one order of magnitude less demanding than competing "end-on" fibre coupling [3, 4]. These factors combine to make grating-couplers an attractive solution for future mass-production and fibre-packaging of commercial Si-photonic circuits and systems.

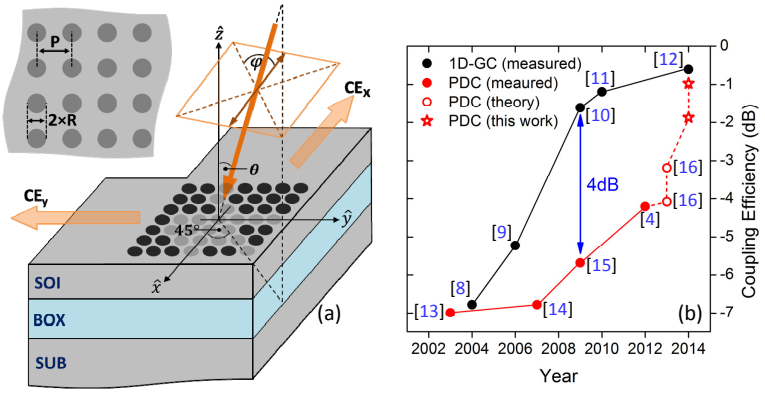

Fig. 1. (a) Schematic of a polarization diversity coupler (PDC) realized in a SOI wafer. The Si-layer is separated from the Si-substrate (SUB) by a bottom-oxide layer (BOX). The hole-radius (R) and grating-pitch (P) of the photonic crystal array (PCA) etched into the Si-layer are shown in the inset. The near-normally incident fibre-mode is projected onto the photonic crystal array of the coupler with an angle-of-incidence of θ, and the polarization angle of the fibre-mode is given by φ. Light is coupled into the two taper-waveguide arms with coupling efficiencies of CE_X and CE_Y, that depend on the SOI-PDC design parameters, and the polarization angle. (b) A representative set of the best coupling efficiency of different SOI grating coupler designs over the last decade. The numbers in square brackets are the relevant reference. The improvements in 1D-GC performance have come from improved designs that exploit thicker Si-layers and/or bottom-reflector elements, and apodization. The "performance gap" between the best 1D-GCs and PDCs was 4dB in 2009. 3D-FDTD optimization of SOI-PDCs closes this gap < 0.5dB.

The simplest grating coupler is a 1D-grating coupler (1D-GC), and is fabricated by partially etching a periodic array of parallel or curved trenches into the Si-layer of the SOI wafer. However, the coupling efficiency of 1D-GCs is strongly dependent on the polarisation of the input fibre-mode, and this is generally unknown and usually unstable for telecom fibres. As a result, simple 1D-GCs are not strong candidates for most practical ICT applications. Even in advanced 1D-GC designs, where both TE- and TM-polarization of the fibre-mode are coupled [5, 6], there exists the challenge of combining the two modes (different polarization-states and group velocity dispersions) to recover a high total coupling efficiency. This problem is addressed by using a polarization diversity coupler (PDC) or 2D-grating coupler, which couples the fibre-mode into a pair of TE-polarized waveguide modes in the SOI-platform, regardless of the fibre-mode polarization. Sharing the same polarization and dispersion, these two coupled modes can be easily combined, or used in symmetric photonic circuits [7].

Figure 1(a) shows the schematic of typical PDC fabricated in an SOI-wafer, and Fig. 1(b) shows measured coupling efficiencies of representative SOI 1D-GC and PDC designs [8–16] from the last decade. The SOI-PDC in Fig. 1(a) consists of a periodic array of cylinders partially etched to a depth of E into the Si-layer of thickness, S. The cylinders have a radius of R, and are separated by a grating pitch of P. This creates a photonic crystal array, with a square footprint matching the footprint of the incident fibre-mode (typically 11μm × 11μm), that has diffractive periodicity in the $\hat{x}$ and $\hat{y}$ directions. The fibre-mode is near-normally incident on the photonic crystal array, and is diffractively-coupled into a pair of (nearly) orthogonal SOI taper waveguides with TE-polarization [17]. As the polarization-state of the fibre-mode varies, the coupling efficiencies into the two taper-waveguides change, but the

#210055 - $15.00 USD Received 14 Apr 2014; revised 13 May 2014; accepted 14 May 2014; published 9 Jun 2014

sum of both contributions remains almost constant, with only a slight variation, termed the polarization dependent loss (PDL). Advanced SOI-PDC designs (by *Luxtera*) can even eliminate the PDL entirely, while retaining high coupling efficiency, by substituting etched-cylinders with more complicated etch-patterns [18].

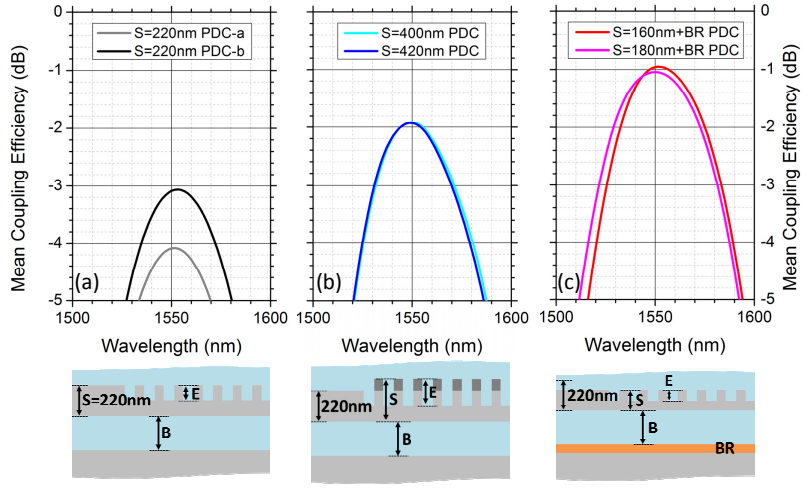

Fig. 2. The coupling efficiency spectra of 3D-FDTD globally optimized PDC designs identified in this work. (a) Coupling spectra of an initial "standard" SOI-PDC design with S = 220nm and E = 70nm (PDC-a = [4]) and after 3D-FDTD optimization (PDC-b = [16]) to identify the optimum etch-depth. The performance gain from 3D-FDTD optimization in 220nm SOI is 1dB. (b) A further 1dB increase in performance is identified for designs with S≈400nm. (c) Yet another 1dB increase in performance is achieved by introducing a metallic bottom-reflector (BR) in the SOI-PDC design. In total, 3D-FDTD optimization of SOI-PDC design brings a total performance boost of 3dB over existing, non-optimized designs, and enables SOI-PDCs to reach the 1dB coupling threshold for the first time. In all cases, the 1dB bandwidth of the SOI-PDCs is ≈40nm, which is sufficient for most multiplexed telecom applications.

While 1D-GC designs can be quickly simulated and optimized using 2D finite difference time domain (2D-FDTD) calculations, computationally–intensive 3D-FDTD calculations are needed to simulate PDCs [16]. Because of this, there has been little progress in optimizing SOI-PDC designs, and this has led to a significant "performance gap" between the coupling efficiencies of 1D-GCs and the PDCs. This point is illustrated in Fig. 1(b), where we plot the improvement in measured coupling efficiencies for representative SOI 1D-GC and PDC designs against time, over the last decade. The significant improvements in 1D-GC performance have come from (i) moving to thicker (S > 220nm) SOI architectures, (ii) using apodized gratings, and (iii) introducing CMOS-compatible bottom-reflector (BR) elements in the design. In 2009, the performance gap between 1D-GC and PDC designs was 4dB. The first full device-scale simulation of a SOI-PDC did not appear until 2013; it used 3D-FDTD simulations to (i) correctly predicted the coupling efficiency of existing 220nm SOI-PDC designs, and (ii) improve the performance of 220nm SOI-PDC designs by 1dB - see Fig. 2(a).

In this article, we show how 3D-FDTD optimization can be taken further, and used to close the "performance gap" between 1D-GCs and PDCs, by identifying new high-performance SOI-PDC designs. As shown in Fig. 2(b), increasing the SOI thickness from S = 220nm to S = 400nm, along with careful tuning of the other design parameters, boosts the coupling performance by 1dB, to give a coupling efficiency of −1.9dB (65%) at 1550nm. A further 1dB performance boost is achieved by introducing a bottom-reflector into the SOI-PDC design, as illustrated in Fig. 2(c). Here, the 1550nm coupling efficiency reaches −0.95dB with a 42nm 1dB bandwidth, making it the first coupler design to combine practically high coupling efficiency (i.e. reaching the −1dB threshold that is typically

#210055 - $15.00 USD Received 14 Apr 2014; revised 13 May 2014; accepted 14 May 2014; published 9 Jun 2014

accepted as the minimum needed for the telecoms market), along with the inherent industrial-scalability and relaxed alignment-tolerance of a grating coupler scheme. As such, our optimized SOI-PDC design with bottom-reflector represents an important step forward for practical Si-photonics. Adding the calculated coupling efficiencies from Figs. 2(b) and 2(c) to the existing data in Fig. 1(b) shows how our 3D-FDTD optimization can close the performance gap between SOI 1D-GC and PDC designs to just 0.5dB. This demonstrates, for the first time, that properly designed SOI-PDCs can perform almost as well as 1D-GCs.

The design parameters of the 3D-FDTD optimized SOI-PDC designs identified in this work are summarized in Table 1. This article describes the coupling-geometry, 3D-FDTD simulations, and optimization-strategy used to identify these designs as high-performance SOI-PDC designs for practical Si-photonic applications.

Table 1. Summary of design parameters for globally optimized SOI-PDC designs

Si-layer Thickness	Etch-Depth	Hole-Radius	Grating-Pitch	BOX Thickness	Bottom-Reflector	Coupling Efficiency	Reference
220nm*	120nm	185nm	635nm	2000nm*	No	-3.2dB(48%)	16
400nm	291nm	167nm	584nm	1900nm	No	-1.9dB(65%)	This work
160nm	80nm	209nm	696nm	2175nm	Yes	-0.95dB(80%)	This work

*Parameters fixed during the 3D-FDTD optimization

2. Description of structures

The 1550nm single-mode telecom fibre has a mean-field diameter of 10.4μm, and is near-normally incident, with an angle-of-incidence of θ = 10°, on the square patch of photonic crystal array illustrated in Fig. 1(a). The slight off-normal incidence geometry suppresses back-reflections into the fibre and provides a directionality to the light coupled into the taper waveguides. The plane-of-incidence for the fibre-mode bisects the PDC at 45°, to ensure a symmetric geometry that minimizes polarization dependent losses. The polarization angle (φ) of the elliptically-polarized fibre-mode rotates in a plane spanned by vectors lying along $-\hat{x}+\hat{y}$ and $\hat{x}-\hat{y}+\hat{z}\sin\theta$ directions. The edge of the square photonic crystal array is typically 11μm long, with the exact dimension (and number of etched holes) depending on the details of the design parameters. The fibre-mode is diffractively coupled into a pair of SOI taper-waveguides that are approximately aligned along the $\hat{x}$ and $\hat{y}$ directions, with coupling efficiencies of CE_X and CE_Y, respectively. The total coupling efficiency is defined as $CE_T = CE_X + CE_Y$. The phase angle of the elliptically polarized fibre-mode does not affect the coupling efficiency, but the polarization angle plays a role. While both $CE_X(\varphi)$ and $CE_Y(\varphi)$ are sensitive functions of the polarization angle, $CE_T(\varphi)$ is essentially constant, exhibiting only a small polarization dependent loss. As shown in [16] and re-confirmed in this work, the mean coupling efficiency (i.e. polarization-averaged coupling efficiency) of the PDC closely corresponds to $CE_T(\varphi = 45°)$. Therefore, during the 3D-FDTD optimization, $CE_T(45°)$ is chosen as the performance-metric by which the different SOI-PDC designs are judged.

Figures 2(a)-2(c) include schematic cross-sections of the SOI-PDC designs optimized by 3D-FDTD. Figure 2(a) shows a cross-section of a "standard" SOI-PDC, such as that characterized in [14] and computationally optimized in [16]. The Si-layer has a fixed height of S = 220nm, a bottom-oxide (BOX) layer or B = 2000nm, a partial etch of E = 70nm or E = 120nm, and the combination of hole-radius and grating-pitch that give the optimum coupling at λ_P = 1550nm. A top-oxide (TOX) layer is added after etching, to support the process flow for other Si-photonic components. This TOX fills the etched holes, and acts to reduce interface losses and back-reflections, because it has a refractive index comparable to the telecom fibre (and the index-matching epoxy used for fibre-packaging). Our simulations assume perfect index-matching between the fibre-mode and the TOX, with a refractive index of n_{Ox} = 1.44, and n_{Si} = 3.47 for all Si-layers. Figure 2(b) shows the cross-section for a SOI-PDC with S > 220nm. In the simulations, the height of the SOI taper waveguides is held at

#210055 - $15.00 USD Received 14 Apr 2014; revised 13 May 2014; accepted 14 May 2014; published 9 Jun 2014

220nm, regardless of the Si-layer thickness of the PCA. This ensures that the coupled light remains single-mode TE-polarized for all designs. This approach has already been successfully demonstrated for 1D-GC designs, where highly localized "thick" patches of amorphous-Si are deposited on top of the standard 220nm SOI-wafer using Si-epitaxy, before carrying-out the etching of the grating coupler [19, 20]. Figure 2(c) shows the cross-section of a SOI-PDC with a bottom-reflector element. In our simulations, the bottom-reflector is modelled as a perfect mirror. In existing 1D-GC designs, real bottom-reflector elements have been realized using an Al layer [6, 12] or a distributed Bragg reflector [21]. The bottom-reflector reduces losses to the Si-substrate, by giving the fibre-mode a "second chance" to pass through diffractive region of the coupler. For SOI-PDC designs with the bottom-reflector, the optimum SOI thickness is found to be $S < 220$nm. By globally "thinning down" the Si-layer with calibrated steam-oxidation and HF-stripping [22], high-quality Si-layers of the necessary thickness have been fabricated from standard 220nm SOI-wafers, and are found to offer lower waveguide losses, and improved waveguide-filter coupling, with respect to 220nm SOI.

3. Description of simulations

The central wavelength (λ_P) and amplitude of the coupling efficiency spectrum depend on the Si-layer thickness (S), the etch-depth (E), the BOX thickness (B), the hole-radius (R), and the grating-pitch (P) of the SOI-PDC design. Imposing the boundary conditions of $\lambda_P = 1550$nm, and $\theta = 10°$, reduces the number of independent design parameters to four - (i) the Si-layer thickness, (ii) the BOX thickness, (iii) the normalized etch-depth (E/S), and (iv) the normalized hole-size (R/P). Since a 3D-FDTD simulation of a single SOI-PDC design takes ≈90 minutes on a moderately fast desktop PC, it is not feasible to exhaustively sweep all four of these parameters to identify the globally optimized design. Instead, we sweep the design parameters of SOI 1D-GC designs using 2D-FDTD simulations (which run ≈1000 times faster than 3D-FDTD simulations) in order to identify high performance combinations of design parameters, and use these combinations as starting values for a much more limited series of 3D-FDTD simulations of the corresponding SOI-PDC designs.

The parameter-space around these starting values is explored by generating ≈25 unique SOI-PDC designs, each using the initial estimate of the Si-layer and BOX thickness, but spanned by different combinations of E/S and R/P values. The coupling efficiency of each design is calculated using 3D-FDTD, with the grating-pitch iteratively adjusted until λ_P of $CE_T(\varphi = 45°)$ converges to 1550 ± 2nm. A contour plot of $CE_T(\varphi = 45°)$ spanned by E/S and R/P can then be built-up, from which the optimum combination of E/S and R/P (for the initial estimates of Si-layer and BOX thickness) can be immediately identified. Next, a small sweep of the BOX thickness around the initial estimate is performed for the SOI-PDC designs with the optimum pair of E/S and R/P values. This identifies the optimized design parameters (E, R, P, and B) of the SOI-PDC with the initial estimate of the Si-layer thickness. When this procedure is repeated for different Si-layer thicknesses around the initial estimated value, i.e. when the design parameter of S is also allowed to vary, then the globally optimized set of all parameters can be identified.

4.1 Optimized designs without bottom-reflector

Figure 3(a) shows the coupling efficiency of 6517 unique SOI 1D-GC designs without bottom-reflector, as calculated by 2D-FDTD simulations. Each design has a unique combination of Si-layer thickness (from $S = 160$nm to 520nm, in 19 steps), BOX-thickness (from $B = 1800$nm to 2100nm, in 7 steps), etch-depth (from $E = 0.2 \times S$ to $0.8 \times S$, in 7 steps), and duty-cycle (from $DC = 0.2$ to 0.8, in 7 steps). Each design is individually centred on $\lambda_P = 1550 \pm 2$nm by tuning the grating-pitch. The hierarchy of the parameter sweep is S-B-E-D, so while the duty-cycle changes for each design, the Si-layer thickness only changes every 343 designs ($343 = 7 \times 7 \times 7$), etc. The parameter sweep identifies the best-performing

#210055 - $15.00 USD Received 14 Apr 2014; revised 13 May 2014; accepted 14 May 2014; published 9 Jun 2014

uniform SOI 1D-GC as having a coupling efficiency of −1.4dB (73%), at S = 420nm. This is in good agreement with measured values of uniform 1D-GC performance with S = 380nm (69%) [10] and apodized 1D-GC performance with S = 340nm (76%) [11].

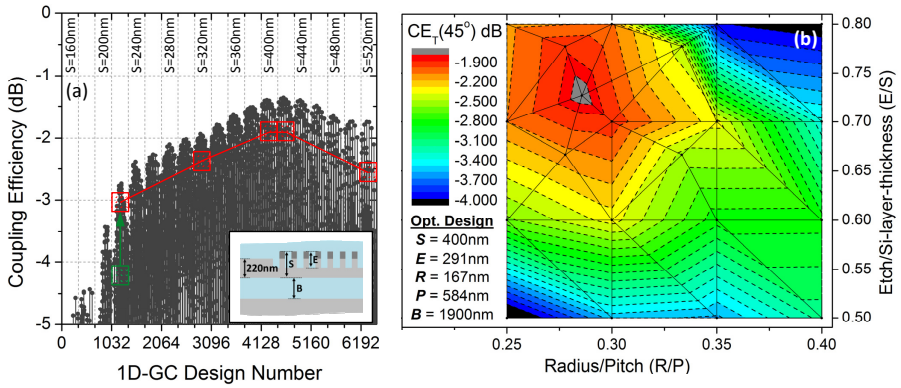

Fig. 3. (a) The coupling efficiency of 6517 SOI 1D-GC designs, each with a unique combination of Si-layer thickness, BOX thickness, etch-depth, and duty-cycle, as calculated by 2D-FDTD simulations. Each coupler is centred on λ_P = 1550 ± 2nm by tuning the pitch. Promising combinations of design parameters identified by this 2D-FDTD sweep are used as starting values for 3D-FDTD simulations of the corresponding SOI-PDCs. The coupling efficiencies of the 3D-FDTD optimized SOI-PDC designs with S = 220nm, 320nm, 400nm, 420nm, and 520nm are indicated by red rectangles, where the height of the rectangles indicates the polarization dependent loss of the design. The performance gap between the best 1D-GC designs and optimized PDC designs is < 0.5dB. (b) The coupling efficiency contour plot of 20 unique SOI-PDC designs, all with S = 400nm and B = 1900nm. The peak of this contour plot corresponds to the globally optimized SOI-PDC design without bottom-reflector, where the optimum combination of E/S = 291nm/400nm and R/P = 167nm/584nm gives a coupling efficiency of −1.9dB = 65%.

The design parameters of the best performing SOI 1D-GC design (S = 420nm, B = 1900nm, E = 252nm, D = 0.7) are used as the starting values for the optimization of the high performance SOI-PDC design. After following the procedure outlined in Section 3, the optimized SOI-PDC design parameters are identified as S = 400nm, B = 1900nm, E/S = 291nm/400nm = 0.73, and R/P = 167nm/584nm = 0.29. As shown in the contour plot of Fig. 3(b), this SOI-PDC design offers a coupling efficiency of −1.9dB (65%), meaning that the performance gap with respect to the best SOI 1D-GC is just 0.5dB. The coupling spectrum of this optimized SOI-PDC design is given in Fig. 2(b), and has a 1dB bandwidth of 38nm, which is adequate for multiplexed telecom applications. To establish if the performance gap can be closed for all Si-layer thicknesses, 3D-FDTD optimization was also carried-out for SOI-PDCs with S = 220nm, 320nm, and 520nm. The red boxes in Fig. 3(a) show the coupling efficiencies of these optimized SOI-PDC designs, where the height of the box indicates the magnitude of the polarization dependent loss (discussed in Section 5). For comparison, the green box in Fig. 3(a) illustrates the measured performance of a non-optimized SOI-PDC design. Clearly, both 1D-GC and PDC designs follow the same general trend, with the performance gap falling to just 0.3dB (53% vs. 50%) for S = 220nm. This demonstrates that properly optimized SOI-PDC designs can perform almost as well as 1D-GC designs.

4.2 Optimized designs with bottom-reflector

Adding a bottom-reflector below the BOX-layer of a SOI 1D-GC is known to substantially increase its coupling efficiency [6, 9, 12]. However, there have been no reports of high performance SOI-PDC designs that incorporate a bottom-reflector element. There have been a limited number of non-SOI PDC designs that use wafer-to-wafer bonding technology to add a

#210055 - $15.00 USD Received 14 Apr 2014; revised 13 May 2014; accepted 14 May 2014; published 9 Jun 2014

bottom-reflector [17], but this approach is costly, and fundamentally not CMOS-compatible. Recent work has shown that it is possible to "locally" deposit metallic patches on the bottom surface of the BOX layer that act as bottom-reflector elements for grating couplers, while maintaining CMOS-compatibility [6, 12]. The scheme is illustrated in Fig. 4(c), where the procedure is as follows: (i) the grating coupler is etched in the SOI-layer using a standard approach, (ii) a TOX layer is added for handling and process-flow, (iii) a dry/wet selective-etch of the Si-substrate is used to open a high-aspect-ratio trench to the underside of the BOX layer, and (iv) a 20µm × 20µm patch of Al is deposited onto the BOX. This Al patch is somewhat larger than the nominal 11µm × 11µm footprint of the coupler, to allow for the alignment tolerances associated with "flipping" the wafer for back-side etching.

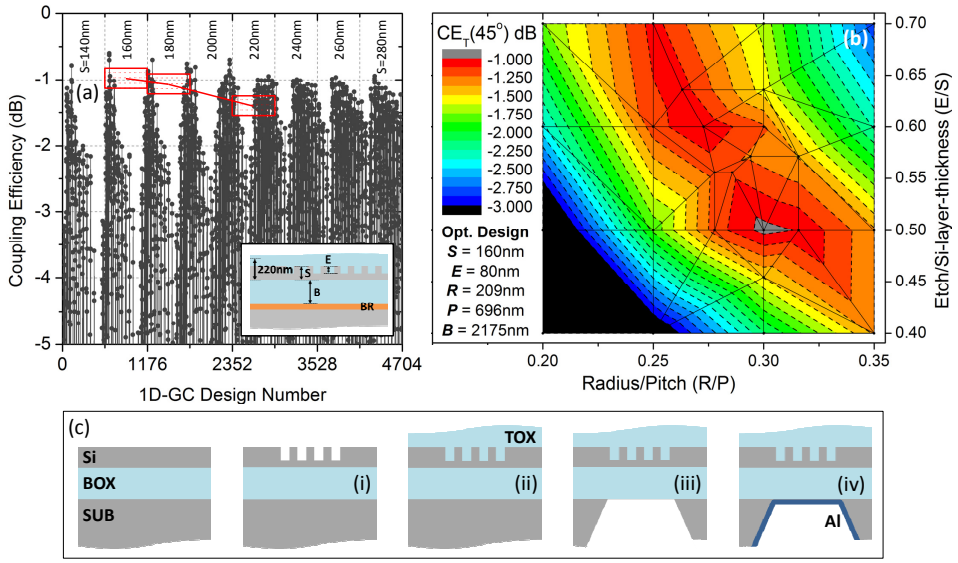

Fig. 4. (a) The coupling efficiency of 4704 SOI 1D-GC designs with bottom-reflector, each with a unique combination of Si-layer thickness, BOX thickness, etch-depth, and duty-cycle, as calculated by 2D-FDTD simulations, all tuned to λ_P = 1550nm. The coupling efficiencies of the 3D-FDTD optimized SOI-PDC designs with bottom-reflectors for S = 160nm, 180nm, and 220nm are indicated by the red rectangles, where the height of the rectangle corresponds to the gives the polarization dependent loss. The performance gap between 1D-GCs and optimized PDCs is < 0.5dB (b) The coupling efficiency contour plot of 25 SOI-PDC designs with bottom-reflector, all with S = 160nm and B = 2175nm. The optimum combination of E/S = 80nm/160nm and R/P = 209nm/696nm gives a coupling efficiency of –0.95dB = 80%. **(c)** A schematic of the CMOS-compatible approach to apply a bottom-reflector element to a SOI-PDC, as described in [6].

Figure 4(a) shows the coupling efficiency of 4704 unique SOI 1D-GC designs with bottom-reflector, as calculated by 2D-FDTD simulations. Each design has a unique combination of Si-layer thickness (from S = 150nm to 290nm, in 8 steps), BOX-thickness (from B = 1550nm to 2100nm, in 12 steps), etch-depth (from $E = 0.2 \times S$ to $0.8 \times S$, in 7 steps), and duty-cycle (from DC = 0.2 to 0.8, in 7 steps). The range of the BOX thicknesses in this sweep spans 550nm (≈1550nm/2n_{OX}) to ensure the identification of a condition for perfectly constructive interference. As was the case in Section 4.1, each 1D-GC design is individually tuned to λ_P = 1550 ± 2nm, and the sweep hierarchy is *S-B-E-D*, so that the Si-layer thickness changes only once every 588 designs (588 = 12 × 7 × 7). The sweep identifies the best-performing uniform SOI 1D-GC with bottom-reflector as having a coupling efficiency of –0.6dB (87%) with S = 170nm, B = 1600nm (or 2150nm), E = 51nm, DC = 0.5, and P = 694nm. This is the highest reported calculated coupling-efficiency for a uniform SOI 1D-GC design with bottom-reflector. However, it is somewhat less than the reported coupling

#210055 - $15.00 USD Received 14 Apr 2014; revised 13 May 2014; accepted 14 May 2014; published 9 Jun 2014

efficiency form calculations of apodized SOI 1D-GC designs with bottom-reflector (−0.45dB = 92%) [9]. Both of these calculations compare well with reports of measured coupling efficiencies of −0.62dB (87%) from apodized SOI 1D-GCs with bottom-reflectors [12].

Using the same optimization procedure as that outlined in the previous section, the parameters for the optimized SOI-PDC design with bottom-reflector are identified as S = 160nm, B = 2175nm, E/S = 80nm/160nm = 0.5, and R/P = 209nm/696nm = 0.3. As shown in the contour plot of Fig. 4(b), this SOI-PDC design offers a coupling efficiency of −0.95dB (80%). The coupling spectrum of this optimized SOI-PDC with bottom-reflector is given in Fig. 2(c), and has a 1dB bandwidth of 42nm. The red boxes in Fig. 4(a) show the coupling efficiencies of optimized SOI-PDC designs with bottom-reflectors for S = 160nm, 180nm, and 220nm. In analogy to designs without bottom-reflectors, the performance gap between the 3D-FDTD optimized SOI-PDC designs and 1D-GC designs is typically less than 0.5dB. Our simulations demonstrate that after suitable optimization, CMOS-compatible SOI-PDC designs can perform at the −1dB level. This is an important result, because it is the performance level that is typically accepted as the minimum needed for industrial adoption. Our −0.95dB SOI-PDC design combines high coupling efficiency, low polarization dependent loss (quantified in Section 5), and the relaxed alignment tolerance of a grating coupler scheme, all while remaining compatible with industrially-scalable 193nm UV-lithography.

In principle, further gains in SOI-PDC coupling efficiency are possible through apodization of the grating structures to create non-uniform designs that better match the fibre-mode profile. However, in our initial investigations of apodized SOI-PDCs, using a genetic algorithm to optimize both the hole-radius and grating-pitch (with S = 220nm, E = 120nm and no bottom-reflector) we only improved the coupling efficiency by 1.5% after 200 hours of 3D-FDTD simulations. It is likely that other SOI-PDC designs (with higher E/S ratios) will show greater performance improvements after apodization. However, the long simulation times needed to perform genetic optimization make such work impractical on a desktop PC.

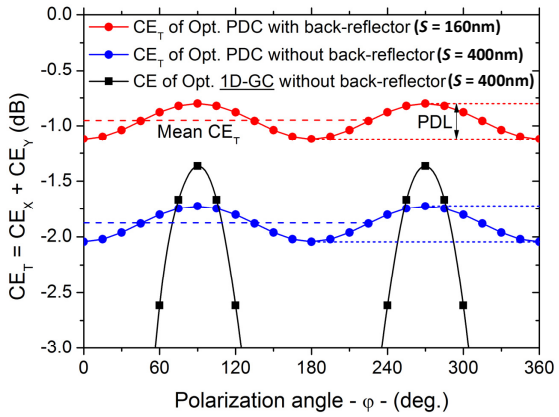

Fig. 5. The variation of total coupling efficiency (CE_T) from the optimized SOI-PDC designs, as a function of fibre-mode polarization angle, as determined by polarization-resolved 3D-FDTD simulations. The polarization dependent loss (PDL) for both designs is 0.3dB. The mean coupling efficiencies of the designs with and without bottom-reflector are −0.95dB and −1.9dB, respectively. These values corresponds almost exactly to corresponding values of $CE_T(\varphi = 45°)$ used as the performance metric during the 3D-FDTD optimization.

5. Effect of fibre-mode polarization and alignment on coupling efficiency

Ideally, the total coupling efficiency ($CE_T = CE_X + CE_Y$) of a PDC would be entirely independent of the fibre-mode polarization. However, the near-normally incident geometry

#210055 - $15.00 USD Received 14 Apr 2014; revised 13 May 2014; accepted 14 May 2014; published 9 Jun 2014

results in a projection of the fibre-mode onto the vertical axis, i.e. the $\hat{z}$ axis in Fig. 1(a), that even a perfectly designed PDC cannot access. As a result, the total coupling efficiency exhibits a slight amplitude variation, termed the polarization dependent loss (PDL) around the mean value, along with a slight "wobble" of about 1nm around the target wavelength of λ_P = 1550nm. The typically ≈40nm 1dB bandwidth of the coupling spectrum is not significantly affected by the fibre-mode polarization. Using polarization-resolved 3D-FDTD simulations, the total coupling efficiency of the optimized designs at λ_P = 1550nm, with and without bottom-reflector elements, can be calculated. As shown in Fig. 5, the PDL for both designs is 0.3dB, with mean coupling efficiencies of −0.95dB and −1.9dB for the designs with and without bottom-reflector, respectively. To provide a comparison, the variation of coupling efficiency from an optimized SOI 1D-GC is also shown in Fig. 5. Although the 1D-GC has a higher maximum coupling efficiency than the corresponding PDC design, it only reaches this level for a very narrow range of fibre-mode polarization.

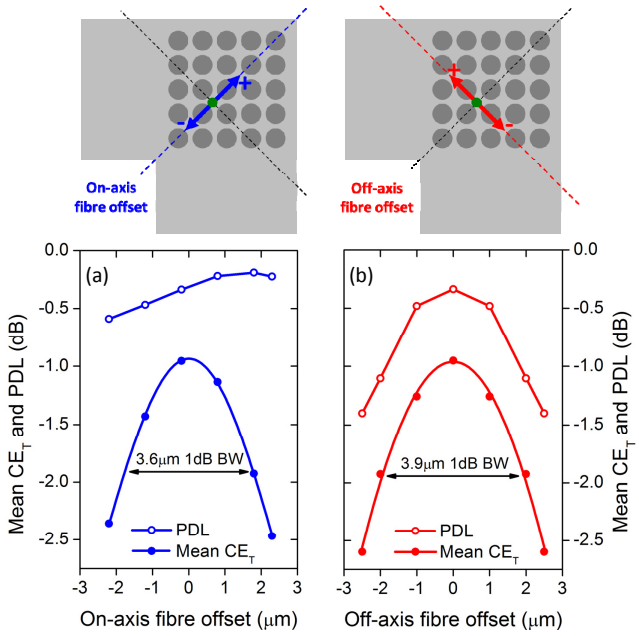

Fig. 6. (a) The effect of fibre alignment on CE_T and PDL for the SOI-PDC design with bottom-reflector design, for a fibre-scan along the symmetry axis of the PDC. The green spot indicates the "sweet spot" of optimum alignment that gives the maximum coupling efficiency of −0.95dB. The mean CE_T has a 1dB alignment tolerance of 3.6μm, and a PDL that is only weakly affected by the fibre-alignment. (b) The effect of fibre alignment on CE_T and PDL for a fibre-scan orthogonal to the symmetry axis of the PDC. The mean CE_T has a 1dB alignment tolerance of 3.9μm, and a PDL that depends sensitively on fibre-position, increases to −1.1dB for an alignment tolerance of ± 2μm.

The alignment tolerance for industrial packaging of the SOI-PDC design with bottom-reflector is estimated from a series of polarization-resolved 3D-FDTD simulations, in which the input fibre-mode is scanned across the surface of the coupler. The PDC has a symmetry axis defined by the plane-of-incidence in Fig. 1(a) and the arms of the taper-waveguides. A fibre-alignment scan along this axis does not reduce the symmetry of the system, and so only weakly affects the PDL, but a scan orthogonal to this axis reduces the overall symmetry and so increases the PDL substantially. As shown in Fig. 6(a), the mean CE_T of the SOI-PDC with bottom-reflector has a 1dB alignment tolerance of 3.6μm along the symmetry axis. As indicated by the green spot in the schematic elements of Fig. 6, the "sweet spot" of optimum

#210055 - $15.00 USD Received 14 Apr 2014; revised 13 May 2014; accepted 14 May 2014; published 9 Jun 2014

alignment is located approximately 1μm from the centre of the PDC. As the fibre-mode is displaced along the symmetry axis, towards the centre of the PDC, the PDL decreases to less than –0.2dB, but increases as the mode is displaced towards the edge of the coupler. As shown in Fig. 6(b), when the fibre-mode is displaced orthogonal to the symmetry axis, the 1dB alignment tolerance is 3.9μm, which is almost identical to that of displacement along the axis. However, for orthogonal fibre-mode displacement, the PDL increases rapidly, because the symmetry of the system is reduced, and reaches –1.1dB for a mode displacement of ± 2μm.

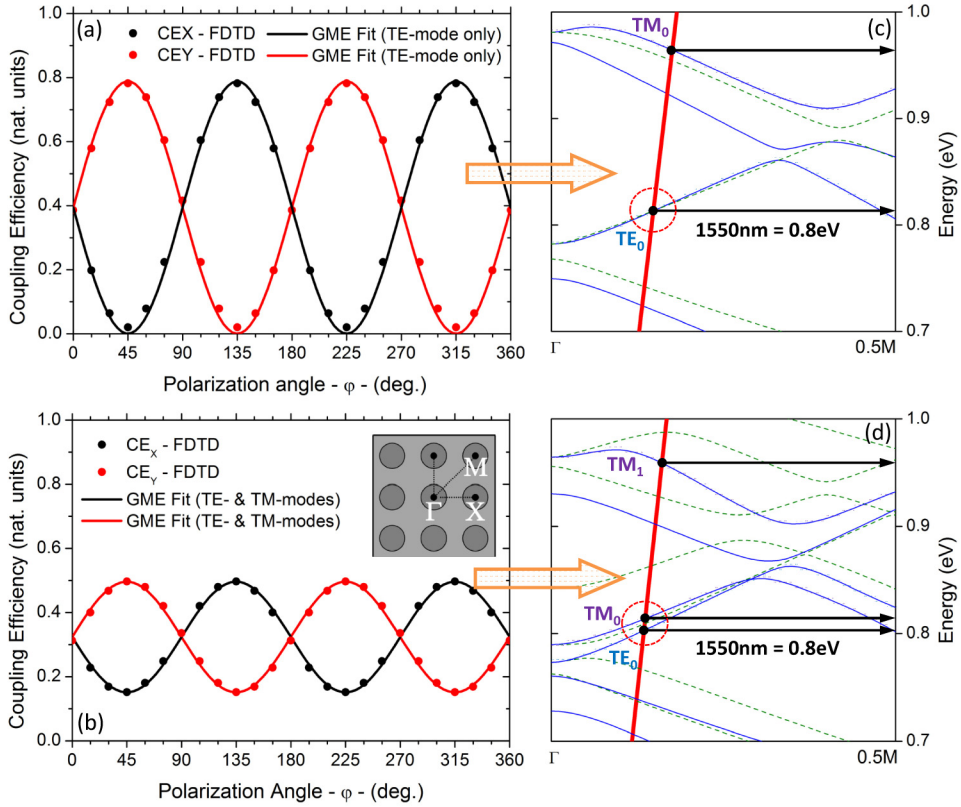

Fig. 7. (a) and (b) The variation of CE_X and CE_Y as a function of the fibre-mode polarization angle of the 3D-FDTD optimized SOI-PDC designs, with and without the bottom-reflector, respectively. The data-points are determined from a series of polarization-resolved 3D-FDTD calculations, and the solid lines are least-square fits based on the results of guided mode expansion calculations and the symmetry of the fibre-mode projection. The inset in (b) shows the coordinates of the reciprocal lattice of the photonic crystal array used in the GME calculations. (c) and (d) The photonic mode dispersion of the (infinitely extended) photonic crystal array in the 3D-FDTD optimized S = 160nm and S = 400nm PDC designs, respectively. The heavy lines indicate dipole-active photonic modes. The heavy blue/purple lines identify the TE/TM-polarization of the modes with respect to the internal geometry of the GME calculation. The almost vertical red line is the "light-line" of the fibre-mode - where it intersects a dipole-active mode, the SOI-PDC has a coupling resonance. The S = 160nm design has a single resonance near λ_P = 1550nm = 0.8eV with a TE-mode, while the S = 400nm design has two, with both a TE-mode and TM-mode. The presence of these different modes at the target wavelength of the coupler explains the different polarization dependence of CE_X and CE_Y observed for the two SOI-PDC designs in (a) and (b).

Although the total coupling efficiency of both PDC designs varies almost identically with the fibre-mode polarization, the variation of the individual coupling efficiencies into the

#210055 - $15.00 USD Received 14 Apr 2014; revised 13 May 2014; accepted 14 May 2014; published 9 Jun 2014

taper-waveguides (i.e. CE_X and CE_Y) behave quite differently. As shown in Figs. 7(a) and 7(b), the S = 160nm PDC design with bottom-reflector behaves as a polarization splitting coupler that offers a high exclusion (≈19dB) between the two waveguides, while the S = 400nm PDC design always couples a significant fraction of the fibre-mode into both waveguides, regardless of its polarization. The origin of these different polarization dependencies, along with an insight into the origin of the diffractive coupling in the SOI-PDC, is given by the photonic mode dispersion of the photonic crystal array at the centre of the coupler.

The dispersion of the (quasi-) guided photonic modes can be estimated by applying the guided-mode expansion (GME) method [23] to the SOI-PDC designs. GME relies on the solution of the stationary Maxwell equations as a linear eigenvalue problem, after expanding the electric and magnetic fields on a basis of modes vertically guided in the layered dielectric structure (i.e. evanescently decaying in the upper and lower cladding layers). Although GME calculations intrinsically assume semi-infinite TOX and BOX layers (i.e. no bottom-reflection contributions), as well as an infinitely-extended photonic crystal array, they have been applied successfully to the interpretation of SOI-PDC designs with S = 220 nm [16]. Figures 7(c) and 7(d) show the GME-calculated quasi-guided mode dispersions around λ_P = 1550nm (E_P = 0.8eV) for the optimized SOI-PDC designs with S = 160nm (with bottom-reflector) and S = 400nm (without bottom-reflector), respectively. The photonic modes are classified with respect to the corresponding guided modes in the basis of the GME calculations, i.e. they can be TE- or TM-polarized with respect to the multi-layered effective planar waveguide of the photonic crystal, with full/dashed lines corresponding to odd/even modes with respect to the vertical mirror plane. Note that these TE/TM classifications are not correlated to the polarization of light coupled into the SOI taper-waveguides; the light coupled into the taper-waveguides remains strongly TE-polarized, regardless of the symmetry or polarization of the photonic band that mediates the coupling. In Figs. 7(c) and 7(d), the nearly vertical red-lines indicate the θ = 10° "light-line" of the incident fibre mode. Where this light-line intersects a dipole-active mode, indicated by heavy blue lines (TE photonic mode) or heavy purple lines (TM photonic mode), the SOI-PDC has a coupling resonance. The number and polarization of these intersections near λ_P = 1550nm = 0.8eV dictate the magnitude and variation of the coupling efficiency into the taper-waveguides as a function of the fibre-mode polarization.

For the optimized SOI-PDC design with bottom-reflector (S = 160 nm), the light-line intersects a single dipole-active mode near 1550nm. The TE_0-mode at this intersection is responsible for the diffractive coupling in this SOI-PDC design. Geometric arguments, based on GME and the symmetry of the projection of the fibre-mode, predict that the coupling efficiencies of this design vary as follows: $CE_X(\varphi) = \left|A\sin(\varphi+45°)\right|^2$ and $CE_Y(\varphi) = \left|A\cos(\varphi+45°)\right|^2$, where φ is the polarization angle defined in Fig. 1(a), and A is a measure of the coupling strength to the dipole-active TE_0-mode. As shown in Fig. 7(a), the values of $CE_X(\varphi)$ and $CE_Y(\varphi)$ from the polarization-resolved 3D-FDTD calculations are well fitted by these trigonometric expressions, with A = 0.89. For the optimized SOI-PDC design without bottom-reflector (S = 400 nm), the thicker silicon layer creates a denser photonic band structure. As shown in Fig. 7(d), the light-line for this SOI-PDC design intersects with both a dipole-active TE_0- and TM_0-mode near 1550nm. This is possible because the thicker Si-layer allows the TM_0 to reach such low energies (the TM_0 resonance is in the S = 160nm design is at 0.96eV = 1290nm). Within the assumptions of GME, the overlap of these two intersection at 1550nm is only approximate, but the 3D-FDTD optimization tunes both of these resonances to precisely 1550nm, as it systematically maximises the total coupling efficiency. For combined TE_0- and TM_0-mode resonances, the geometric GME arguments predicts that the coupling efficiencies depend on the fibre-mode polarization as follows: $CE_X(\varphi) = \left|A\sin(\varphi+45°)+B\cos(\varphi+45°)\right|^2$ and

#210055 - $15.00 USD Received 14 Apr 2014; revised 13 May 2014; accepted 14 May 2014; published 9 Jun 2014

$CE_Y(\varphi) = \left|A\cos(\varphi+45°) + B\sin(\varphi+45°)\right|^2$, where A and B are now coupling strengths to the active TE_0- and TM_0- modes, respectively. As shown in Fig. 7(b), the polarization-resolved FDTD calculations match the trigonometric expressions well, with A = 0.705, and $B = 0.389e^{i93°}$, confirming the physical origin of the coupling process.

Conclusion

We have shown that 3D-FDTD calculations can be used to identify high performance 1550nm SOI-PDC designs, with and without bottom-reflector elements, by globally optimizing the design parameters of Si-layer thickness, etch-depth, grating-pitch, hole-radius, and BOX-layer thickness. This approach allows for the bridging of the performance gap between SOI-PDC designs and SOI 1D-GC designs, closing the gap to less than 0.5dB. For optimized SOI-PDC designs without bottom-reflector, increasing the Si-layer thickness to S = 400nm allows for a coupling efficiency of −1.9dB. The optimized SOI-PDC design with CMOS-compatible bottom-reflector reaches a coupling efficiency of −0.95dB, has a 1dB bandwidth of 42nm, offers a low polarization dependent losses of 0.3dB (± 3.5%), and has a 1dB alignment tolerance of 3.6μm. Offering high coupling efficiency, low polarization dependent loss, and the inherently relaxed alignment tolerances of a grating coupler, our optimized SOI-PDC design reaches the −1dB performance threshold needed for real-world ICT applications.

Acknowledgments

The authors are grateful to A. Fincato for emphasising the importance of reaching the −1dB threshold for industrial adoption. The authors also acknowledge useful discussions on fabrication tolerances with C. Lacava.

#210055 - $15.00 USD Received 14 Apr 2014; revised 13 May 2014; accepted 14 May 2014; published 9 Jun 2014